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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

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Examiner: Edgardo Ortiz

Group Art Unit: 2815

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For: FIELD EFFECT TRANSISTOR  
HAVING A DOPED GATE  
ELECTRODE WITH REDUCED GATE  
DEPLETION AND METHOD OF  
FORMING THE TRANSISTOR

**APPEAL BRIEF**

**MS APPEAL BRIEF - PATENTS**

Commissioner of Patents  
P.O. Box 1450  
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I hereby certify that this correspondence is being deposited with the U.S. Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the date below:

September 8, 2005  
Date

*Mary Paul*  
Signature

Sir:

Applicants hereby submit this Appeal Brief to the Board of Patent Appeals and Interferences in response to the Final Office Action dated June 14, 2005. The Notice of Appeal for this application was filed on July 13, 2005.

**The Director is authorized to deduct the fee for filing this Appeal Brief (\$500) from Advanced Micro Devices, Inc. Deposit Account No. 01-0365/DE0347.<sup>1</sup>**

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<sup>1</sup> In the event the monies in that account are insufficient, the Director is authorized to withdraw funds from Williams, Morgan & Amerson, P.C. Deposit Account No. 50-0786/2000.110600.

**I. REAL PARTY IN INTEREST**

The present application is owned by Advanced Micro Devices, Inc.

**II. RELATED APPEALS AND INTERFERENCES**

Applicants are not aware of any related appeals and/or interferences that might affect the outcome of this proceeding.

**III. STATUS OF THE CLAIMS**

1-15 and 21-32 are pending in the application. Claims 1-15 and 21-32 were rejected in the Final Office Action issued on June 14, 2005. Claims 1-15 and 21-32 are the subject of the present appeal. Claims 1-15 and 21-32 are attached as Appendix A.

**IV. STATUS OF AMENDMENTS**

No amendments have been filed subsequent to the Final Office Action.

**V. SUMMARY OF CLAIMED SUBJECT MATTER**

In general, the present invention is directed to a field effect transistor having a doped gate electrode with reduced gate depletion and a method of forming the transistor. There are three independent claims at issue in the current appeal: claims 1, 22 and 25.

Independent claim 1 is generally directed to a method of forming a field effect transistor that involves forming an implantation mask 220 over a crystalline semiconductor region 204, forming a drain region and a source region adjacent the implantation mask 220, the drain and source regions each having a top surface located above a top surface of the crystalline semiconductor region 204, removing the implantation mask 220 to expose a surface area of the top surface of the crystalline semiconductor region 204, forming a gate insulation layer 206 on

the exposed surface area of the top surface of the crystalline semiconductor region 204, forming a gate electrode 205 on the gate insulation layer 206, and doping the gate electrode 206. This invention is generally described throughout the specification. By way of example only, at least portions of the invention are described at p. 11, l. 3 – p. 20, l. 6; p. 23, ll. 11-22; and Figures 2a-2i..

Independent claim 22 is generally directed to a field effect transistor 200 comprising a substrate having formed thereon a semiconductor region 204 having a top surface, a drain region formed on the top surface of the semiconductor region 204 and extending along a lateral direction and a height direction, a source region 208 formed on the top surface of the semiconductor region and extending along the lateral direction and the height direction, and a gate electrode 205 formed above the top surface of the semiconductor region and extending along the lateral direction and the height direction, the gate electrode 205 laterally located between the drain region 208 and the source region 208 and separated from the top surface of the semiconductor region 204 by a gate insulation layer 206, the drain and source regions 208 extending along the height direction at least to an upper surface of the gate electrode 205. This invention is generally described throughout the specification. By way of example only, at least portions of the invention are described at p. 11, l. 3 – p. 20, l. 6; p. 23, ll. 11-22; and Figures 2a-2i..

Independent claim 25 is generally directed to a method of forming a field effect transistor that involves forming a recess 320a in a semiconductor layer 304, the recess 320a having a bottom surface, forming an implantation mask 320 in at least the recess 320a, forming a drain region and a source region by performing at least one ion implantation process to implant ions into the semiconductor layer 304 adjacent the implantation mask 320, wherein the implantation

mask 320 substantially prevents ions from penetrating the bottom surface of the recess 320a, removing the implantation mask 320 to expose the bottom surface of the recess 320a, forming a gate insulation layer 306 on the exposed bottom surface of the recess 320a, forming a gate electrode on the gate insulation layer, and doping the gate electrode. This invention is generally described throughout the specification. By way of example only, at least portions of the invention are described at p. 20, l. 8 – p. 23, l. 22 and Figures 3a-3e.

## **VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL**

1. Claims 1-4, 9-15, 21-23 and 25-31 stand rejected under 35 U.S.C. § 102(b) as allegedly being anticipated by Chan (U.S. Patent No. 6,252,277).

2. Claims 5-8 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Chan in view of Applicant's admitted prior art (Figures 1a-1d and pages 1-8 of the specification).

3. Claim 24 stands rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Chan in view of Gardner (U.S. Patent No. 6,355,955).

## **VII. ARGUMENT**

### **A. Legal Standards**

As the Board well knows, an anticipating reference by definition must disclose every limitation of the rejected claim in the same relationship to one another as set forth in the claim. *In re Bond*, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990). To the extent the Examiner relies on principles of inherency in making the anticipation rejections in the Office Action, inherency requires that the asserted proposition necessarily flow from the disclosure. *In re Oelrich*, 212 U.S.P.Q. 323, 326 (C.C.P.A. 1981); *Ex parte Levy*, 17 U.S.P.Q.2d 1461, 1463-64 (Bd. Pat. App.

& Int. 1990); *Ex parte Skinner*, 2 U.S.P.Q.2d 1788, 1789 (Bd. Pat. App. & Int. 1987); *In re King*, 231 U.S.P.Q. 136, 138 (Fed. Cir. 1986). It is not enough that a reference could have, should have, or would have been used as the claimed invention. “The mere fact that a certain thing may result from a given set of circumstances is not sufficient.” *Oelrich*, at 326, quoting *Hansgirk v. Kemmer*, 40 U.S.P.Q. 665, 667 (C.C.P.A. 1939); *In re Rijckaert*, 28 U.S.P.Q.2d 1955, 1957 (Fed. Cir. 1993), quoting *Oelrich*, at 326; see also *Skinner*, at 1789. “Inherency ... may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient.” *Skinner*, at 1789, citing *Oelrich*. Where anticipation is found through inherency, the Office’s burden of establishing *prima facie* anticipation includes the burden of providing “...some evidence or scientific reasoning to establish the reasonableness of the examiner’s belief that the functional limitation is an inherent characteristic of the prior art.” *Skinner* at 1789.

Moreover, to establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant’s disclosure. *In re Vaeck*, 947 F.2d 488, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991); M.P.E.P. § 2142. Moreover, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 U.S.P.Q. 580 (CCPA 1974). If an independent claim is nonobvious under 35

U.S.C. § 103, then any claim depending therefrom is nonobvious. *In re Fine*, 837 F.2d 1071, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988); M.P.E.P. § 2143.03.

With respect to alleged obviousness, there must be something in the prior art as a whole to suggest the desirability, and thus the obviousness, of making the combination. *Panduit Corp. v. Dennison Mfg. Co.*, 810 F.2d 1561 (Fed. Cir. 1986). In fact, the absence of a suggestion to combine is dispositive in an obviousness determination. *Gambro Lundia AB v. Baxter Healthcare Corp.*, 110 F.3d 1573 (Fed. Cir. 1997). The mere fact that the prior art can be combined or modified does not make the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F.2d 680, 16 U.S.P.Q.2d 1430 (Fed. Cir. 1990); M.P.E.P. § 2143.01. The consistent criterion for determining obviousness is whether the prior art would have suggested to one of ordinary skill in the art that the process should be carried out and would have a reasonable likelihood of success, viewed in the light of the prior art. Both the suggestion and the expectation of success must be founded in the prior art, not in the Applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991); *In re O'Farrell*, 853 F.2d 894 (Fed. Cir. 1988); M.P.E.P. § 2142.

**B. Claims 1-4, 9-15, 21-23 and 25-32 are Allowable Over the Prior Art of Record**

**1. Claims 1-4, 9-15 and 21**

The Examiner's anticipation rejection of independent claim 1, and all claims depending therefrom, should be reversed. Independent claim 1 is a method claim that recites, among other things, that the drain and source regions are formed adjacent the implantation mask, that the implantation mask is removed to expose a top surface of the crystalline semiconductor region and that the gate insulation layer is formed on the exposed surface of the top surface of the crystalline semiconductor region.

In the Final Office Action, the Examiner asserted that Chan disclosed “forming drain and source regions (39) adjacent said implantation mask (37) (figure 4E), said drain and source regions (39) each having a top surface located above a top surface of said crystalline semiconductor region (30) (figure 4E).” Final Office Action, p. 2. Applicants respectfully assert that the Examiner’s decision is based upon a misunderstanding or misreading of Chan and/or the subject matter defined by claim 1.

In the embodiment relied upon by the Examiner, Chan discloses forming a trench 36 (see Figure 4B) in the substrate 30. An undoped layer of silicon dioxide 37 is deposited above the wafer, as shown in Figure 4C. Col. 4, ll. 39-44. Thereafter, the layer 37 is subjected to a polishing process. Col. 4, ll. 46-51. The oxide layer 37 and the doped oxide layer 32 are removed with a dilute HF acid etch process until the silicon is exposed. A portion of the layer 37 remains positioned in the trench 36 after this process. Col. 4, l. 51 – Col. 5, l. 6; Figure 4D. Then, a selective epitaxial growth process is performed to form doped source/drain element 39. Col. 5, ll. 7-17; Figure 4E.

It is clear from the express disclosure of Chan that the layers 32 and 37 are removed from above the top surface of the substrate prior to the formation of epitaxial silicon source/drain regions 39 that are selectively grown over the exposed silicon regions 38. Col. 5, ll. 7-8. Thus, it is unclear where in Chan the Examiner finds support for the assertion that the epitaxial silicon regions 39 in Chan are formed adjacent the implantation mask 37 that remains positioned in the trench 36. The source/drain regions 39 in Chan are not formed adjacent to the implantation mask 37, as identified by the Examiner. The source/drain regions in Chan are offset from the “implantation mask” 37 by the width of the spacers 35. Independent claim 1 specifically recites that the drain and source regions are formed adjacent the implantation mask. Chan does not

disclose at least this limitation of claim 1. Thus, the Examiner's anticipation rejection of claims 1-4, 9-15 and 21 should be reversed for at least this reason.

Additionally, independent claim 1 recites the step of removing the implantation mask to expose a surface area of a top surface of the crystalline semiconductor region, and forming a gate insulation layer on the exposed surface area of the top surface of the crystalline semiconductor region. In Chan, the gate insulation layer, *i.e.*, the gate oxide 44, is formed on the exposed silicon surface within the trench 36, *i.e.*, on the exposed bottom surface of the trench 36. Thus, claim 1 is not anticipated by Chan for at least this additional reason. It is believed that the Examiner contends that the bottom surface of the trench 36 in Chan is the same as the "top surface" of the semiconductor region set forth in independent claim 1.

It is respectfully submitted that the Examiner's equating of the bottom surface of the trench with the top surface of the semiconductor region is (1) contrary to the teachings set forth in the specification of the present application and (2) contrary to what one skilled in the art would understand the top surface of the semiconductor region to be. Claim 1 is directed to the embodiment depicted in Figures 2a-2i. As shown therein, the semiconductor region or layer 204 has a substantially planar top surface. Thus, to construe the bottom surface of the trench 36 in Chan to be a "top surface" of the semiconductor region would be inconsistent with a specifically disclosed embodiment in the specification. Moreover, it is believed that the Examiner's attempt to equate the bottom surface of the trench 36 in Chan with the top surface of the semiconductor layer in claim 1 is contrary to the understanding of those skilled in the art. It defies logic to assert that, when starting with a material having a substantially planar top surface, as does the wafer 30 depicted in Chan (see Figure 3), the bottom surface of a trench formed in the wafer 30



would also be understood to be a “top surface” of that wafer. For at least this additional reason, it is believed that the Examiner erred in rejecting claims 1-4, 9-15 and 21.

## 2. Claims 25-32

The Examiner also erred in rejected method claims 25-32 as being anticipated by Chan. Independent claim 25 recites forming a recess in a semiconductor layer, forming an implantation mask in at least the recess, forming a drain region and a source region by performing at least one ion implantation process to implant ions into the semiconductor layer adjacent the implantation mask, wherein the implantation mask substantially prevents ions from penetrating the bottom surface of the recess, removing the implantation mask to expose the bottom surface of the recess, forming a gate insulation layer on the exposed bottom surface of the recess, forming a gate electrode on the gate insulation layer and doping the gate electrode. It is respectfully submitted that claims 25-32 are not anticipated by Chan.

In rejecting claims 25-32, the Examiner relied upon the embodiment depicted in Figures 6A-6K in Chan. Final Office Action, pp. 5-6. In rejecting these claims, the Examiner also failed to recognize that Chan does not disclose at least the limitation of performing an ion implant process to form the source/drain regions by implanting ions adjacent the implantation mask. The Examiner identified the layer 37 as the implantation mask. Final Office Action, p. 5; *see, e.g.*, Figures 6C-6D. In Chan, an ion implant process is performed (see Figure 6E) to form source/drain regions 139. However, these implant regions are not implanted adjacent the “implantation mask” 137. The implanted ions are spaced apart from the “implantation mask” 137 by the width of the spacers 135. Thus, the Examiner erred in rejecting claims 25-32 for at least this reason.

**3. Claims 22-24**

Independent claim 22 recites that the drain and source regions are formed on the top surface of the semiconductor region, that the gate electrode is formed above the top surface of the semiconductor region and that the gate electrode is separated from the top surface of the semiconductor region by a gate insulation layer. It is respectfully submitted that Chan does not disclose or suggest the invention set forth in independent claim 22. As set forth above, the gate electrode 47 disclosed in Chan is not formed above a top surface of the semiconductor region nor is it separated from the top surface of the semiconductor region by a gate insulation layer. Accordingly, it is respectfully submitted that the anticipation rejection of independent claim 22, and all claims depending therefrom, should be withdrawn.

**C. Claims 5-8 are Allowable Over the Prior Art of Record**

Dependent claim 5 further recites that a first implantation sequence for forming the source/drain regions is performed prior to epitaxially growing the semiconductor layer, and a second implantation process for forming the source/drain regions is performed after epitaxially growing the semiconductor layer. This claimed methodology is not disclosed nor suggested in the art of record. If anything, Chan, the Examiner's primary reference, teaches away from the method recited in claim 5. In Chan, the epitaxially grown N-type source/drain elements 39 are in situ doped with arsenic during the grow process to form the source/drain regions 39. Col. 5, ll. 7-10. The Examiner concedes that Chan does not disclose the limitations set forth in claim 5. Final Office Action, p. 8. Despite this concession, the Examiner magically concludes that it would have been obvious to arrive at the invention set forth in claim 5 based upon a combination of Chan and Applicants' admitted prior art. In doing so, the Examiner committed reversible error.

If anything, Chan can be said to teach away from the invention set forth in dependent claim 5. Chan discloses a process whereby an *in situ* doping process is used during the epitaxial growth process used to form the source/drain regions 39 disclosed therein. The Examiner does not provide any reason why one skilled in the art would be motivated to ignore the express teachings of Chan regarding this issue and perform two additional ion implantation steps to introduce dopant material to form the source/drain regions – one before epi growth and one after epi growth. Such additional steps would be time-consuming and expensive. Thus, a person of ordinary skill in the art, who are pressured to be reasonable and practical, would not be motivated to modify the teachings of Chan so as to arrive at Applicants' invention.

A recent Federal Circuit case makes it crystal clear that, in an obviousness situation, the prior art must disclose each and every element of the claimed invention, and that any motivation to combine or modify the prior art must be based upon a suggestion in the prior art. *In re Lee*, 61 U.S.P.Q.2d 143 (Fed. Cir. 2002). Conclusory statements regarding common knowledge and common sense are insufficient to support a finding of obviousness. *Id.* at 1434-35. It is respectfully submitted that the Examiner's assertion that dependent claim 5 would have been obvious in view of the combination of Chan and Applicants' admitted prior art is based upon an improper use of hindsight using Applicants' disclosure as a roadmap. Accordingly, it is respectfully submitted that dependent claim 5, and all claims depending therefrom, are in condition for immediate allowance.

### **VIII. CLAIMS APPENDIX**

The claims that are the subject of the present appeal – claims 1-15 and 21-32 – are set forth in the attached "Claims Appendix."

**IX. EVIDENCE APPENDIX**

There is no separate Evidence Appendix for this appeal.

**X. RELATED PROCEEDINGS APPENDIX**

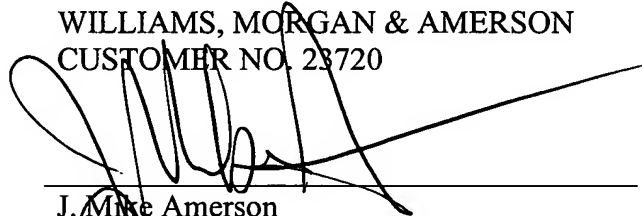
There is no Related Proceedings Appendix for this appeal.

**XI. CONCLUSION**

In view of the foregoing, it is respectfully submitted that the Examiner erred in not allowing claims 1-15 and 21-32 over the prior art of record. Applicants respectfully request the Board reverse the Examiner's rejections. The undersigned attorney may be contacted at (713) 934-4055 with respect to any questions, comments or suggestions relating to this appeal.

Respectfully submitted,

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## **APPENDIX A**

1. A method of forming a field effect transistor, the method comprising:  
forming an implantation mask over a crystalline semiconductor region;  
forming a drain region and a source region adjacent said implantation mask, said drain and source regions each having a top surface located above a top surface of said crystalline semiconductor region;  
removing said implantation mask to expose a surface area of said top surface of said crystalline semiconductor region;  
forming a gate insulation layer on said exposed surface area of said top surface of said crystalline semiconductor region;  
forming a gate electrode on said gate insulation layer; and  
doping said gate electrode.
2. The method of claim 1, wherein forming said gate electrode includes depositing a gate electrode material above said gate insulation layer and removing excess material of said gate electrode material to form the gate electrode.
3. The method of claim 1, wherein a lateral size of said implantation mask is greater than a design value of a gate length of said gate electrode.
4. The method of claim 1, wherein forming said drain and source regions adjacent said implantation mask includes epitaxially growing a crystalline semiconductor layer adjacent to said implantation mask.

5. The method of claim 4, wherein a first implantation sequence for forming said drain and source regions is performed prior to epitaxially growing the semiconductor layer and a second implantation sequence for forming said drain and source regions is performed after epitaxially growing the semiconductor layer.

6. The method of claim 5, further comprising performing an anneal process to activate said dopants.

7. The method of claim 6, wherein said anneal process is controlled on the basis of a desired channel length defined by a lateral distance of the drain region and the source region.

8. The method of claim 7, wherein said anneal process includes a first anneal cycle performed after said first implantation sequence and prior to said second implantation sequence, said first anneal cycle being configured to substantially completely re-crystallize amorphized portions in said semiconductor region.

9. The method of claim 3, further comprising forming sidewall spacers on sidewalls of said drain and source regions that are exposed by removing said implantation mask.

10. The method of claim 9, wherein a width of said sidewall spacers is controlled on the basis of a target gate length for said gate electrode.

11. The method of claim 1, wherein said implantation mask is removed by an isotropic etch process.

12. The method of claim 2, wherein said excess material is removed by chemical mechanical polishing.

13. The method of claim 2, wherein said excess material is removed by an etch process.

14. The method of claim 2, wherein said excess material is removed by chemical mechanical polishing and etching.

15. The method of claim 1, further comprising forming metal/semiconductor compound regions on said gate electrode and said drain and source regions.

21. The method of claim 1, wherein said doping of the gate electrode is performed on the basis of process parameters selected to restrict dopant penetration of the gate insulation layer.

22. A field effect transistor, comprising:

a substrate having formed thereon a semiconductor region having a top surface;

a drain region formed on said top surface of said semiconductor region and extending along a lateral direction and a height direction;

a source region formed on said top surface of said semiconductor region and extending along said lateral direction and said height direction; and

a gate electrode formed above said top surface of said semiconductor region and extending along said lateral direction and said height direction, said gate electrode laterally located between said drain region and said source region and separated from said top surface of said semiconductor region by a gate insulation layer, said drain and source regions extending along said height direction at least to an upper surface of said gate electrode.

23. The field effect transistor of claim 22, wherein said gate electrode is at least partially comprised of a doped semiconductor material, whereby a peak concentration of dopants in said gate electrode is less than a peak concentration of dopants in said drain and source regions.

24. The field effect transistor of claim 23, wherein said semiconductor region is formed on an insulating layer and has an extension in the height direction in the range of approximately 5-50 nm.

25. A method of forming a field effect transistor, the method comprising:

forming a recess in a semiconductor layer, said recess having a bottom surface;

forming an implantation mask in at least said recess;

forming a drain region and a source region by performing at least one ion implantation process to implant ions into said semiconductor layer adjacent said implantation



mask, wherein said implantation mask substantially prevents ions from penetrating said bottom surface of said recess;

removing said implantation mask to expose said bottom surface of said recess;

forming a gate insulation layer on said exposed bottom surface of said recess;

forming a gate electrode on said gate insulation layer; and

doping said gate electrode.

26. The method of claim 25, wherein forming said gate electrode includes depositing a gate electrode material above said gate insulation layer and removing excess material of said gate electrode material to form the gate electrode.

27. The method of claim 25, further comprising, prior to forming said gate insulation layer, forming sidewall spacers on sidewalls of said recess that are exposed by removing said implantation mask.

28. The method of claim 27, wherein a width of said sidewall spacers is controlled on the basis of a target gate length for said gate electrode.

29. The method of claim 25, wherein said implantation mask is removed by an isotropic etch process.

30. The method of claim 25, further comprising forming metal/semiconductor compound regions on said gate electrode and said drain and source regions.

31. The method of claim 25, wherein a lateral dimension of said recess is greater than a target gate length of said gate electrode.

32. The method of claim 25, wherein said recess is formed by anisotropically etching said semiconductor layer.